CLAIMS

What is claimed is:

	1) A prog	grammable comparator for allowing a frequency synthesizer to function	
2	despite long delays comprising:		
	a)	a first phase comparator, the first phase comparator having a first input, a	
4		second input, a third input, and an output;	
	b)	a second phase comparator, the second comparator having a first input, a	
6		second input, a third input, and an output;	
	c)	a programmable dead zone delay circuit, the programmable dead zone	
8		delay circuit having at least a control input, a data input and a data output;	
	d)	a first control circuit, the first control circuit having at least a first input, a	
10		second input, a third input, a first output and a second output;	
	e)	a first NFET, the first NFET having a gate, drain, and a source;	
12	f)	a second NFET, the second NFET having a gate, drain, and a source;	
	g)	wherein the third input of the first phase comparator is driven to a	
14		predetermined logical value by the first output of the first control circuit;	
	h)	wherein the third input of the second phase comparator is driven to a	
16		predetermined logical value by the second output of the first control	
		circuit;	
18	i)	wherein a first signal is applied to the first input of the first phase	
		comparator and the first input of the second phase comparator;	

j) wherein a second signal is applied to the data input of the programmable 20 dead zone delay circuit and the second input of the second phase 22 comparator; k) wherein the output of the programmable dead zone delay circuit is connected to the second input of the first phase comparator; 24 l) wherein the first control input of the programmable dead zone delay circuit 26 controls the time delay of the programmable dead zone delay circuit; m) wherein the output of the first phase comparator is connected to the gates 28 of the first and second NFETs; n) wherein the drain of the first NFET is connected to the output of the 30 second phase comparator; o) wherein the drain of the second NFET is connected to the third input of the 32 second phase comparator; p) wherein the sources of the first and second NFETs are connected GND. 34 2) The circuit as in Claim 1 wherein the first signal is a system clock and the second 2 signal is a delayed system clock. 3) The circuit as in Claim 2 wherein the first phase comparator comprises: 2 a) a first inverter, the first inverter having an input and an output; b) a second inverter, the second inverter having an input and output; 4 c) a third inverter, the third inverter having an input and output; d) a fourth inverter, the fourth inverter having an input and output; e) a third NFET, the third NFET having a gate, source, and drain; 6

f) a fourth NFET, the fourth NFET having a gate, source, and drain; 8 g) wherein the output of the first inverter is connected to the gate of the third NFET; 10 h) wherein the source of the third NFET is connected to the drain of he fourth NFET; 12 i) wherein the source of the fourth NFET is connected to GND; wherein the input of the first inverter is the first input of the first phase 14 comparator; k) wherein the gate of the fourth NFET is the second input of the first phase 16 comparator; 1) wherein the input of the second inverter is connected to the output of the 18 third inverter, the input of the fourth inverter, and the drain of the second NFET; 20 m) wherein the output of the second inverter is the third input of the first phase comparator; 22 n) wherein the output of the fourth inverter is the output of the first phase comparator. 24 26 4) The circuit as in Claim 3 wherein the second phase comparator comprises: 2 . a) a fifth inverter, the fifth inverter having an input and output; b) a sixth inverter, the sixth inverter having a input and output; c) a seventh inverter, the seventh inverter having a input and output; d) a eight inverter, the eight inverter having a input and output;

- e) a fifth NFET, the fifith NFET having a gate, source, and drain; 6 f) a sixth NFET, the sixth NFET having a gate, source, and drain; 8 g) wherein the output of the fifth inverter is connected to the gate of the fifth NFET; h) wherein the source of the fifth NFET is connected to the drain of he sixth 10 NFET; 12 i) wherein the source of the sixth NFET is connected to GND; j) wherein the input of the fifth inverter is the first input of the second phase 14 comparator; k) wherein the gate of the sixth NFET is the second input of the second phase 16 comparator; 1) wherein the input of the sixth inverter is connected to the output of the 18 seventh inverter, the input of the eight inverter, and the drain of the fifth NFET; 20 m) wherein the output of the sixth inverter is the third input of the second phase comparator; 22 n) wherein the output of the eighth inverter is the output of the second phase comparator. 24 5) The circuit as in Claim 4 wherein the programmable dead zone delay circuit 2 comprises a programmable delay line.
 - 6) A circuit as in Claim 5 wherein the first control circuit comprises:
- a) an NOR logic gate, the NOR logic gate having a set of inputs, and an output;

4 b) a seventh NFET, the seventh NFET having a gate, source, and drain; c) a eighth NFET, the eighth NFET having a gate, source, and drain; 6 d) wherein the output of the NOR logic gate is connected to the gate of the seventh NFET and the gate of the eighth NFET; 8 e) wherein the source of the seventh NFET and the source of the eighth NFET are connected to GND: 10 f) wherein the set of inputs of the NOR logic gate is the input to the first control circuit; 12 g) wherein the drain of the seventh NFET is the first output of the first control circuit; 14 h) wherein the drain of the eighth NFET is the second output of the first control circuit. 16 7) A method of manufacturing a programmable comparator for allowing a frequency 2 synthesizer to function despite long delays comprising: a) fabricating a first phase comparator, the first phase comparator having a 4 first input, a second input, a third input, and an output; b) fabricating a second phase comparator, the second comparator having a 6 first input, a second input, a third input, and an output; c) fabricating a programmable dead zone delay circuit, the programmable 8 dead zone delay circuit having at least a control input, a data input and a data output; 10 d) fabricating a first control circuit, the first control circuit having at least a

first input, a second input, a third input, a first output and a second output;

e) fabricating a first NFET, the first NFET having a gate, drain, and a source;

12

f) fabricating a second NFET, the second NFET having a gate, drain, and a 14 source; g) wherein the third input of the first phase comparator is driven to a predetermined logical value by the first output of the first control circuit; 16 h) wherein the third input of the second phase comparator is driven to a 18 predetermined logical value by the second output of the first control circuit; 20 wherein a first signal is applied to the first input of the first phase comparator and the first input of the second phase comparator; 22 wherein a second signal is applied to the data input of the programmable dead zone delay circuit and the second input of the second phase 24 comparator; k) wherein the output of the programmable dead zone delay circuit is 26 connected to the second input of the first phase comparator; l) wherein the first control input of the programmable dead zone delay circuit 28 controls the time delay of the programmable dead zone delay circuit; m) wherein the output of the first phase comparator is connected to the gates 30 of the first and second NFETs; n) wherein the drain of the first NFET is connected to the output of the 32 second phase comparator; o) wherein the drain of the second NFET is connected to the third input of the 34 second phase comparator;

p) wherein the sources of the first and second NFETs are connected GND.

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- 8) The method as in Claim 7 wherein the first signal is a system clock and the second signal is a delayed system clock.
 - 9) The method as in Claim 8 wherein the first phase comparator comprises:
- a) a first inverter, the first inverter having an input and an output;
 - b) a second inverter, the second inverter having an input and output;
- c) a third inverter, the third inverter having an input and output;
 - d) a fourth inverter, the fourth inverter having an input and output;
- e) a third NFET, the third NFET having a gate, source, and drain;
 - f) a fourth NFET, the fourth NFET having a gate, source, and drain;
- g) wherein the output of the first inverter is connected to the gate of the third NFET;
- h) wherein the source of the third NFET is connected to the drain of he fourth NFET;
- i) wherein the source of the fourth NFET is connected to GND;
 - j) wherein the input of the first inverter is the first input of the first phase comparator;
 - k) wherein the gate of the fourth NFET is the second input of the first phase comparator;
 - wherein the input of the second inverter is connected to the output of the third inverter, the input of the fourth inverter, and the drain of the second NFET;
- m) wherein the output of the second inverter is the third input of the first phase comparator;

22	n)	wherein the output of the fourth inverter is the output of the first phase
		comparator.
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	10) The cir	rcuit as in Claim 9 wherein the second phase comparator comprises:
2	a)	a fifth inverter, the fifth inverter having an input and output;
	b)	a sixth inverter, the sixth inverter having a input and output;
4	c)	a seventh inverter, the seventh inverter having a input and output;
	d)	a eight inverter, the eight inverter having a input and output;
6	e)	a fifth NFET, the fifith NFET having a gate, source, and drain;
	f)	a sixth NFET, the sixth NFET having a gate, source, and drain;
8	g)	wherein the output of the fifth inverter is connected to the gate of the fifth
		NFET;
10	h)	wherein the source of the fifth NFET is connected to the drain of he sixth
		NFET;
12	i)	wherein the source of the sixth NFET is connected to GND;
	j)	wherein the input of the fifth inverter is the first input of the second phase
14		comparator;
	k)	wherein the gate of the sixth NFET is the second input of the second phase
16		comparator;
	1)	wherein the input of the sixth inverter is connected to the output of the
18		seventh inverter, the input of the eight inverter, and the drain of the fifth
		NFET;
20	m)	wherein the output of the sixth inverter is the third input of the second

phase comparator;

n) wherein the output of the eighth inverter is the output of the second phase 22 comparator. 24 11) The method as in Claim 10 wherein the programmable dead zone delay circuit comprises a programmable delay line. 12) A method as in Claim 11 wherein the first control circuit comprises: a) an NOR logic gate, the NOR logic gate having a set of inputs, and an 2 output; 4 b) a seventh NFET, the seventh NFET having a gate, source, and drain; c) a eighth NFET, the eighth NFET having a gate, source, and drain; 6 d) wherein the output of the NOR logic gate is connected to the gate of the seventh NFET and the gate of the eighth NFET; 8 e) wherein the source of the seventh NFET and the source of the eighth NFET are connected to GND; 10 f) wherein the set of inputs of the NOR logic gate is the input to the first control circuit; g) wherein the drain of the seventh NFET is the first output of the first 12 control circuit; h) wherein the drain of the eighth NFET is the second output of the first 14 control circuit. 16